FET POWER PERFORMANCE PREDICTION USING A LINEARIZED DEVICE MODEL

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Abstract

A new model has been developed which, based on a linearized device model, describes the power output at 1 dB gain compression, optimum load impedance and load-pull contours of a FET explicitly in terms of device parameters. Applications of the model to practical devices including commercial MESFET's and a 0.25um-gate MODFET showed agreement with measurements to 40GHz.

Introduction

There exist two types of models used for predicting the power performance of a FET device in class A operation. Empirical/graphical models have been widely accepted for many applications [1] [2], but they do not describe the frequency dependence of power performance or tend not to make quantitatively accurate predictions over a wide range of frequencies. Numerical models, although potentially very accurate [3]-[9], are apt to give only device specific results and to fail in providing a global and generalized view of device power performance.

A new analytical model developed and described in this paper predicts the power output at 1 dB gain compression, optimum load impedance for power and load-pull contours of a device from its linearized model with reasonable accuracy and directly relates the performance to device parameters.

Model Description

Fig. 1 defines the linearized device model proposed for power performance prediction. A dc I-V characteristic of a FET is a simplification from a measured one with four boundaries of operation defined as drain-voltage limits of V_{knee} and V_{BR} and gate-voltage limits (drain-curent limits) of V_{GL} and V_{GH}. The device is linearized within an area enclosed by the boundaries and is represented by a small-signal equivalent circuit for a chosen DC bias condition of V_D and V_G. This choice of equivalent circuit guarantees model agreement with measurements at low power levels. The value of g_m is assumed to be null beyond the gate-voltage limits.

When a device shows a reasonably high gain, the equivalent circuit in Fig. 1 can be approximated by the one shown in Fig. 2, for which a simple circuit analysis yields a relation between ac voltage and current.

$$|v_d| = |i_d| \cdot \frac{|R + Z_L|}{|1 + (g_{ds} + j\omega C_{ds}')(R + Z_L)|} \qquad (1)$$

where $|i_d| = g_m|v_{gs}|$ and $R = R_s + R_d$. The device inductance $L_d + L_s$, is treated as a part of the load impedance, Z_L, for analysis simplicity.

Power saturation is assumed to be predominantly invoked by a compression of either gm or effective device output resistance with an increased signal level when a trajectory of i_d or v_d reaches one of the respective operation boundaries to cause wave form compression. As derived from Eq. (1), the v_d and i_d boundaries will be reached simultaneously if a Z_L satisfies the following equation.

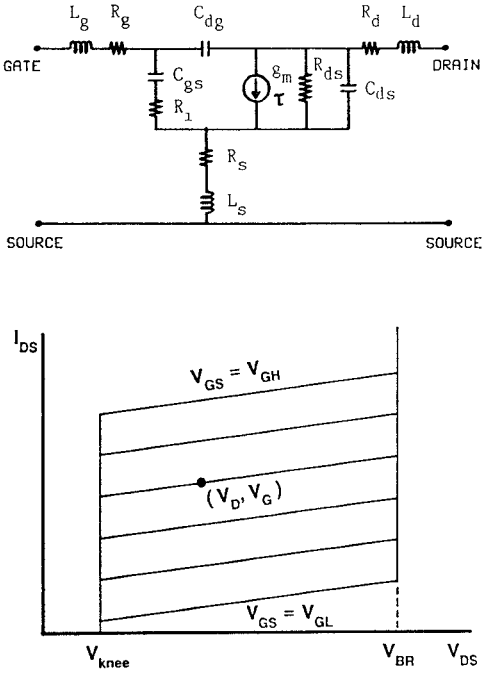

Fig.1 Linearized device model for predicting power Performance. A device is represented by a small-signal equivalent circuit at a bias point chosen for power operation. The element designation follows general convention. The DC I-V characteristics is a simplification from a measured one.

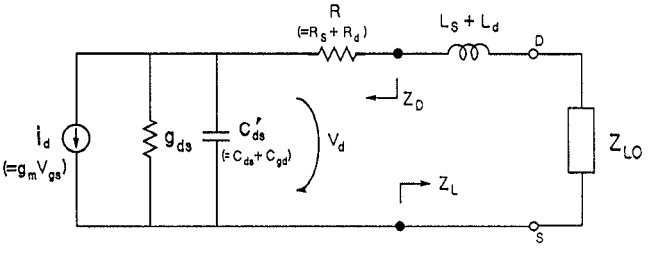

Fig.2 Simplified device model for its output performance. The Z_{LO} is an external load impedance to the device.

$$\frac{|Z_L + Z_D|}{|Z_L + R|} = \frac{|Y_D|_{max}}{|g_{ds} + j\omega C_{ds}'|} \qquad (2)$$

where $Z_D = R + 1/(g_{ds} + j\omega C_{ds}')$

$|Y_D|_{max} = |i_d|_{max} / |v_d|_{max} = g_m |v_{gs}|_{max} / |v_d|_{max}$

$|v_{gs}|_{max} = Min[\, |V_G - V_{GL}|, |V_G - V_{GH}| \,]$

and $|v_d|_{max} = Min[\, |V_D - V_{knee}|, |V_D - V_{BR}| \,]$

and Z_D is the device output impedance. Eq. (2) expresses an Apollonius circle in a Z_L plane (see Fig. 4) and demarcates two regions according to power saturation mechanism.

Region 1) gate-voltage limited power saturation:

When a load impedance Z_L is in the region which includes the origin of the Z_L plane, a drain voltage will never exceed $|v_d|_{max}$ even for the maximum gate voltage $|v_{gs}|_{max}$. Thus the power saturation is caused by the gate voltage limit, for which an expression of output power, P_L, is derived simply by calculating a mismatch loss to the device output impedance.

$$P_L = \frac{\alpha |i_d|^2_{max}}{|g_{ds} + j\omega C_{ds}'|^2} \cdot \frac{Re\, Z_L}{|Z_L + Z_D|^2} \qquad (3)$$

where α is 0.5 for maximum linear power and 0.78 for power at 1 dB gain compression as will be discussed later.

i) If the complex conjugate of Z_D, Z_D^*, is within the gate-voltage limited region, or if

$$|Y_D| = \frac{\sqrt{g_{ds}^2 + (\omega C_{ds}')^2} \cdot [2R\{g_{ds}^2 + (\omega C_{ds}')^2\} + 2g_{ds}]}{\sqrt{[2R\{g_{ds}^2 + (\omega C_{ds}')^2\} + g_{ds}]^2 + (\omega C_{ds}')^2}} \geq |Y_D|_{max} \qquad (4)$$

then P_L is maximized to P_{Lmax} when a Z_L is conjugately matched to the device output impedance.

$$P_{Lmax} = \frac{\alpha |i_d|^2_{max}}{|g_{ds} + j\omega C_{ds}'|^2} \cdot \frac{1}{4\, Re\, Z_D} \qquad (5)$$

where $Z_{Lopt} = Z_D^*$

Thus, the optimum load for power, Z_{Lopt}, coincides with the optimum load for small-signal gain. Eq. (4) will be more easily satisfied at higher frequencies since $|Y_D|$ monotonically increases with frequency.

ii) If Z_D^* is not within the gate-voltage limited region then the maximum power is obtained for a Z_L along the boundary circle given by Eq. (2) since Eq. (3) is a monotonically decreasing function of Z_L around Z_D^*. An application of Lagrange multipliers to Eqs. (2) and (3) leads to the optimum load as a solution to the following simultaneous equations.

$$\begin{cases} (r + r_D)^2 + (x + x_D)^2 = A[(r + R)^2 + x^2] \\ 2xr[r + r_D - A(r + R)] = (Ax - x - x_D)(R^2 - r^2 + x^2) \end{cases} \qquad (6)$$

where $Z_{Lopt} = r + jx$, $Z_D = r_D + jx_D$

and $A = |Y_D|^2_{max} / |g_{ds} + j\omega C_{ds}'|^2$

and

$$P_{Lmax} = \frac{\alpha |i_d|^2_{max}}{|g_{ds} + j\omega C_{ds}'|^2} \cdot \frac{Re\, Z_{Lopt}}{|Z_{Lopt} + Z_D|^2} \qquad (7)$$

$$= \alpha |v_d|^2_{max} \frac{Re\, Z_{Lopt}}{|Z_{Lopt} + R|^2}$$

Region 2) drain-voltage limited power saturation:

When a load Z_L is in the region which includes an infinite impedance in the Z_L plane, a drain voltage reaches $|v_d|_{max}$ for a gate voltage less than $|v_{gs}|_{max}$. The power saturation is thus invoked by the drain voltage limit, for which the output power is calculated by Eq. (8).

$$P_L = \alpha |v_d|^2_{max} \frac{Re\, Z_L}{|Z_L + R|^2} \qquad (8)$$

Eq. (8) takes the absolute maximum when $Z_L = R$ and decreases monotonically around it. Since for almost all practical FETs the resistance R is outside the drain-voltage limited region unless $|Y_D|_{max} \geq (1 + 2Rg_{ds})/(2R)$, the maximum output power is again obtained for a Z_L along the boundary circle, resulting in Eqs. (6) and (7).

Therefore, if Z_D^* is not in the gate-voltage limited region of a Z_L plane, the maximum output power is always achieved for a Z_L which causes the gate voltage and drain-voltage limits to be reached simultaneously.

Eq. (6) can be solved approximately if $|Y_D|_{max}$ is much greater than g_{ds} and $\omega C_{ds}'$ and if $|Y_D|_{max} << 1/R$, leading to device output equivalent circuit for power matching shown in Fig. 3. $|Y_D|_{max}$ is virtually identical to a classical load resistance [1]. The effective capacitance, however different from the Cripps model [2], is about 20-30% higher than a device capacitance C_{ds}' for a typical FET due to a finite value of g_{ds}.

A load-pull contour of a device is defined as a constant output power contour in a Z_L plane for a fixed level of input power corresponding to the P_{Lmax}. Since $|v_{gs}|^2_{max}$ or $|i_d|^2_{max}$ well represents the input power level, a load-pull contour in the gate-voltage limited region is directly expressed by Eq. (3), thus coinciding with a small-signal gain (or mismatch loss) contour circle with respect to Z_D^*. The varying Z_L in the drain-voltage limited region on the other hand causes deeper compression of a drain voltage, leading to Eq. (9) as an expression for a load-pull contour. The equation was obtained by substituting $|v_d|_{fund}$ for $|v_d|_{max}$ in Eq. (8), where $|v_d|_{fund}$ is the amplitude of the fundamental frequency component in the compressed drain waveform.

$$\frac{Re\, Z_L}{|Z_L + R|^2} = \left[\frac{|v_d|_{max}}{|v_d|_{fund}}\right]^2 \cdot \frac{P_L}{\alpha |v_d|^2_{max}} \qquad (9)$$

A zero-th order approximation that $|v_d|_{max} / |v_d|_{fund} = 1$ will predict a contour circle narrower than an actual measured contour. Fig. 4 graphically illustrates Eqs. (3) and (9).

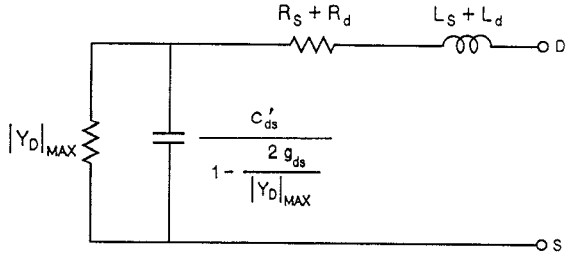

Fig.3 An approximate output equivalent circuit of an FET for power matching when $g_{ds} << |Y_D|_{max} << 1/R$ and $\omega C_{ds}' << |Y_D|_{max}$.

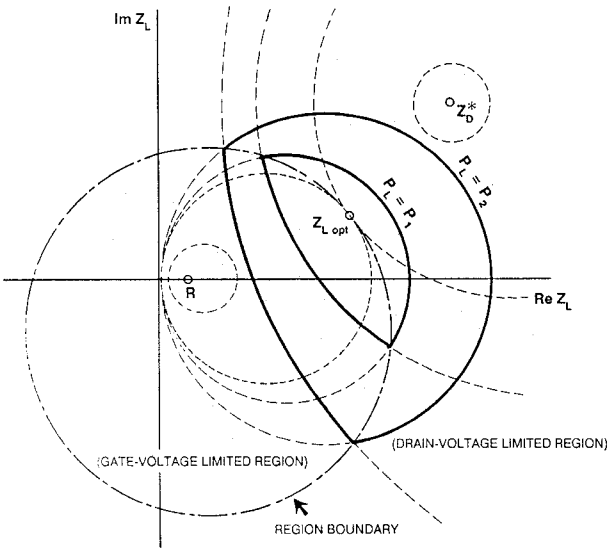

Fig.4 Graphical representation of the predicted load-pull contours of an FET device. The contours in the drain-voltage limited region are of the zero-th order approximation. The figure shows a case where Z_D^* is in the drain-voltage limited region. The region boundary circle of Eq.(2) is drawn by a sigle dotted line.

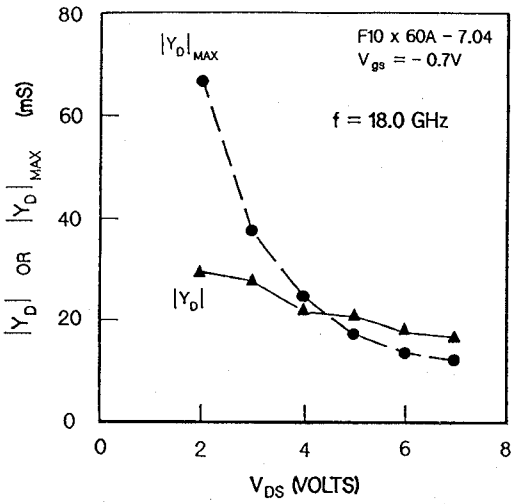

Fig.5 The calculated $|Y_D|$ and $|Y_D|_{max}$ at 18GHz for a 0.5μm-gate ion-implanted MMIC MESFET as a function of drain bias voltage.

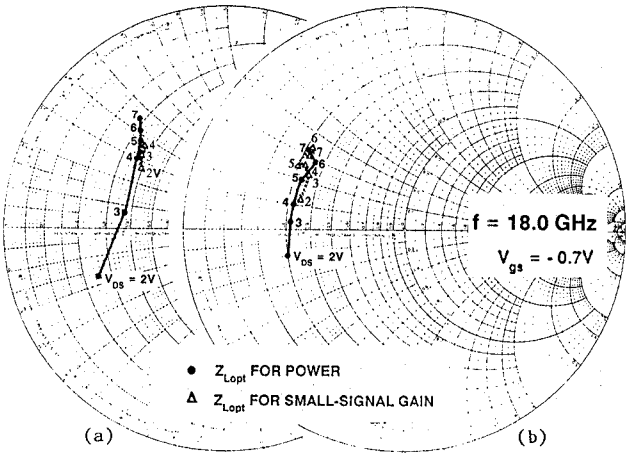

Fig.6 (a) The predicted optimum loads for power and small-signal gain for the MESFET of Fig.5, compared with (b) measured results.

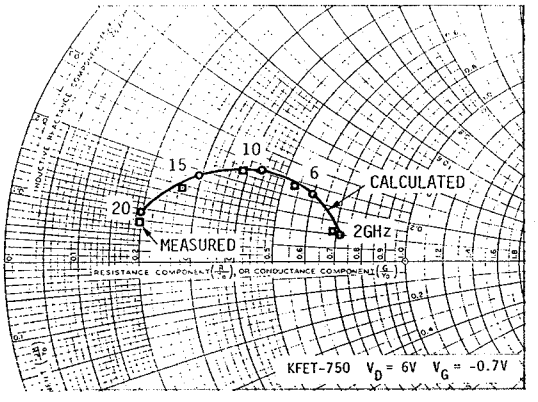

Fig.7 Comparison of the calculated and measured optimum loads for power for a pulse-doped HP MESFET over a 2-20GHz frequency range.

Experiments

Measurements have been performed on five types of FET's for their power and load-pull characteristics using a system described in Reference [10]. Small-signal equivalent circuits of the devices were determined from measured S-parameters using the algorithm explained in Reference [11]. The value of $|V_{gs}|_{max}$ for the power performance calculation was defined as a gate voltage swing at which a geometric average of g_m becomes 85% of a small-signal g_m at a DC bias point. The value of α was chosen to be 0.78 for calculating power at 1 dB gain compression, based on an analysis of the first order approximation that the power saturation is due to abrupt clipping of gate and drain voltages.

Fig. 5 shows the $|Y_D|_{max}$ and $|Y_D|$ of Eq. (4) calculated at 18 GHz for 0.5 um-gate ion-implanted HP MESFET as a function of drain bias voltage V_{DS}. The calculation predicts that the optimum load for power and the optimum load for small-signal gain coincide for a V_{DS} greater than 4.5V and that they separate apart further with the lowered drain voltage. The measured optimum loads are plotted in Fig. 6, showing a good agreement with this prediction.

Fig. 7 shows the calculated optimum load for power for a 0.3 um-gate HP MESFET over a 2-20 GHz frequency range,which favorably compares with measured results. The device is a pulse-doped MESFET with 750 um gate periphery capable of delivering 26 dBm output power at 18 GHz. Table 1 compares the measured and calculated output power for this device along with the ion-implanted MESFET and three other devices investigated.

Fig. 8 plots the calculated load-pull contours of the Harris HMF-2400, NEC710 and the 0.25 um-gate HP MODFET listed in Table 1 at 7 GHz, 25 GHz and 25 GHz, respectively. Good agreement can be observed with measured results. Further experiment on the MODFET to 40 GHz also indicated good agreement with its model within measurement accuracy.

Conclusion

A new analytical model has been developed which, based on a linearized device model, describes the power at 1 dB gain compression, optimum load for power, and load-pull contours of a FET explicitly in terms of device parameters. Its applications to practical

Table 1. Comparison of the measured and calculated output power

DEVICE	GATE WIDTH W_g (μm)	DC BIAS M V_D V_G	FREQ. (GHz)	POWER AT 1dB GAIN COMPRESSION (dBm) (meas.)	(cal.)
HP MESFET (ion-implanted)	600	6 -0.7	18	22.0	21.8
HP MESFET (pulse-doped)	750	6 -0.7	18	25.7	26.4
Harris HMF-2400	2400	8 -1.2	7	30.6	31.2
NEC710	280	5 -0.4	25	20.9	21.1
HP MODFET	360	5 -0.7	25	20.5	20.7

devices demonstrated the validity of the model by showing good agreement with measurements. Although this work has exclusively investigated common-source FET's, the model should be also applicable to common-gate FET's and to the other types of devices such as bipolar transistors with minor modifications.

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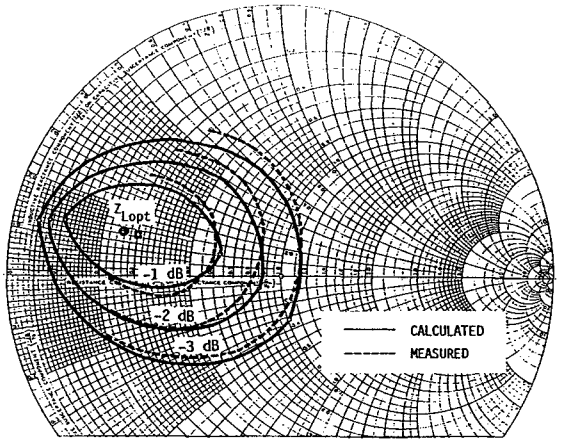
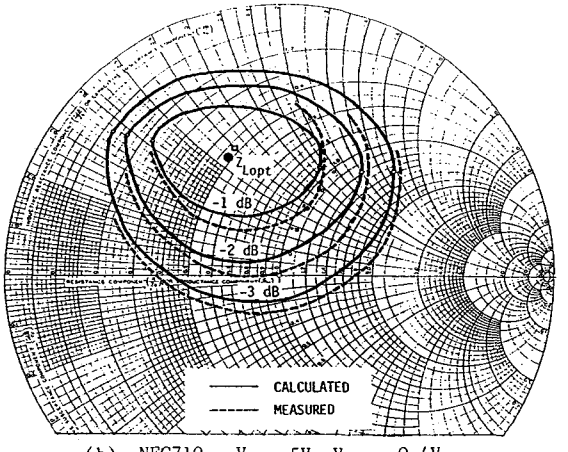
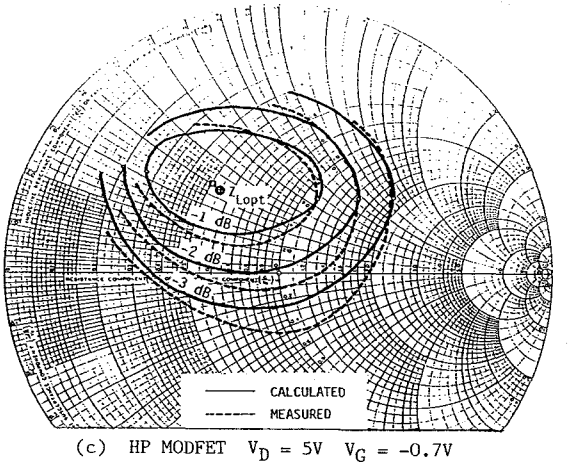


(a) HMF-2400 V_D = 8V V_G = -1.2V



(b) NEC710 V_D = 5V V_G = -0.4V



(c) HP MODFET V_D = 5V V_G = -0.7V

Fig.8 The calculated load-pull contours compared with measurement for (a) Harris HMF-2400 at 7GHz, (b) NEC710 at 25GHz and (c) 0.25μm-gate MODFET at 25GHz.